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(54) **Data processing network**

(57) In a data processing network having a plurality of data processing stations 11 communicating over a bus 10 with each station inductively coupled 12 to the bus data is transmitted in a binary coded form in which a zero is represented by a pair of oppositely poled pulses and a one is represented by the absence of any pulse. The transmitter circuit includes an energy saving circuit for recoverying energy from the backswing of each pulse. Preferably the bus consists of a twisted pair of wires.

Each station is coupled to the bus by a core with two transmittets windings. Each winding is connected in series with a respective capacitor. The capacitors are charged through a diode circuit and are selectively discharged through the windings to generate the pulses on the bus. A separate receive core is provided.

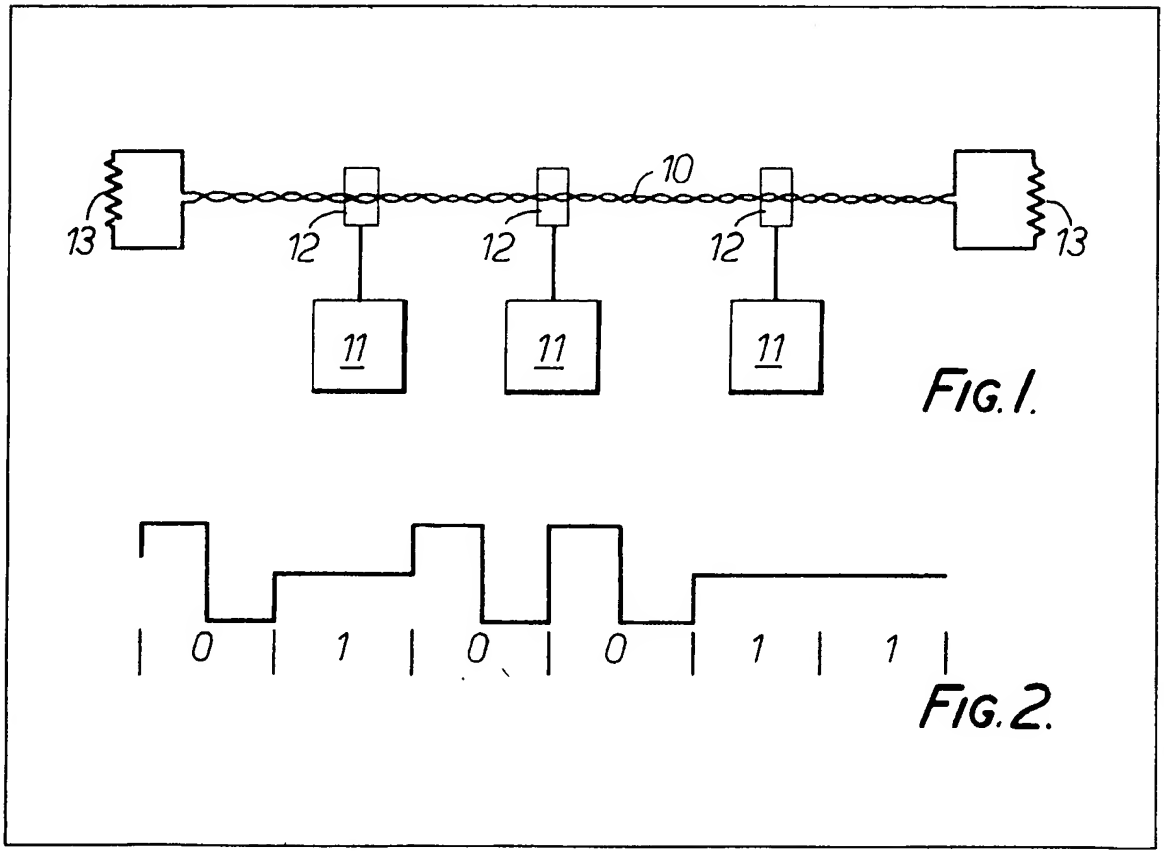

FIG. 1.

FIG. 2.

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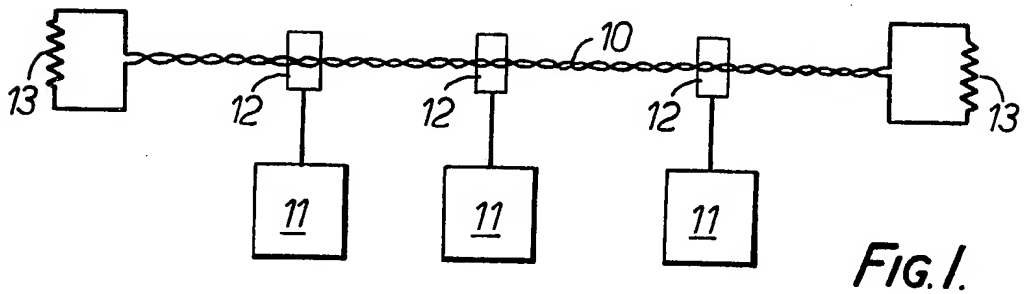

FIG. 1.

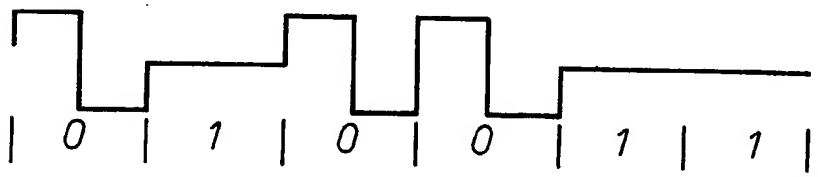

FIG. 2.

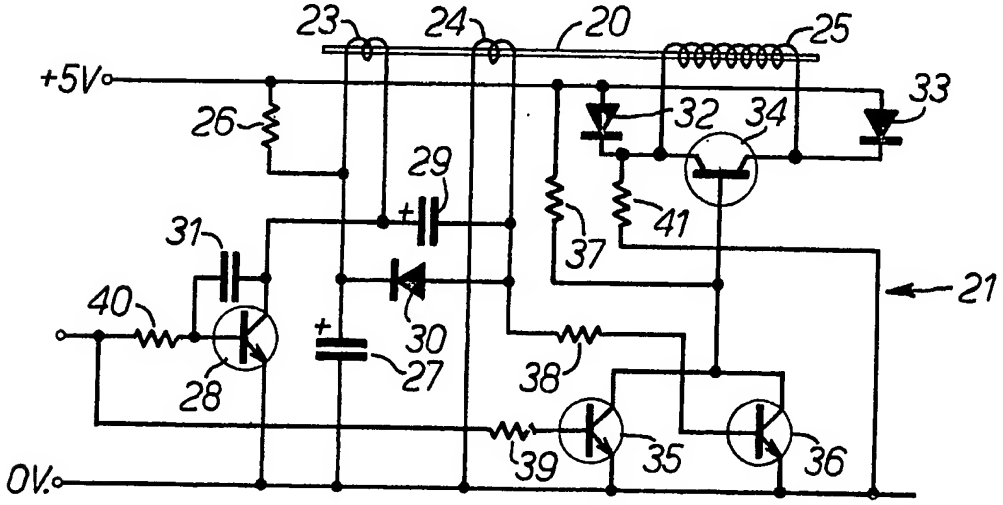

FIG. 3.

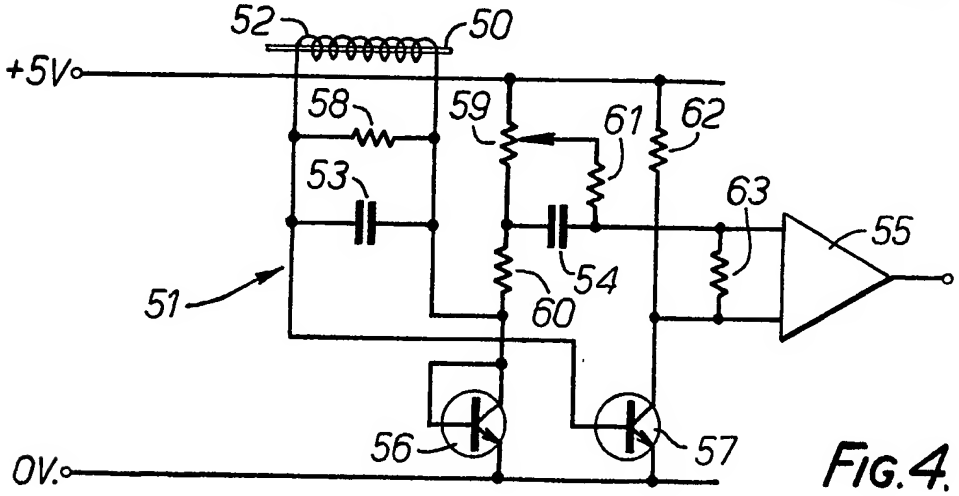

FIG. 4.

SPECIFICATION

Data processing network

Background to the invention

This invention relates to data processing networks comprising a plurality of data processing stations which can communicate with each other over a common bus.

One such network is described for example in U.S. Patent No. 4063220 in which the common bus is a co-axial cable and in which connections are made to the bus by forming T-junctions in the cable. Another such network is described in U.S. Patent No. 4199663 in which the bus is a twisted pair of wires and connections are made inductively by means of magnetic cores, threaded through the twisted pair. The advantage of this is that it is not necessary to cut the bus or to remove any insulation from the wires in order to make a connection.

A problem with inductive coupling is that it may be difficult to ensure that the cores are connected to the bus in the correct sense. If they are connected in the wrong sense, the transmitted signals will be inverted and this may prevent correct transmission of the data. Another problem is that if the signal on the bus has a net D.C. component, this may lead to an undesirable build-up of voltage.

One object of the present invention is to overcome these problems.

Summary of the invention

According to the invention there is provided a data processing network comprising:-

(a) a plurality of data processing stations;

(b) a common bus interconnecting the stations; and

(c) means for inductively coupling each station to the bus to allow the stations to communicate with one another over the bus;

(d) wherein each station has transmitter means for transmitting data over the bus in a binary-coded form in which one bit value is represented by a pulse immediately followed by a pulse of opposite polarity, and the other bit value is represented by the absence of any pulse.

It can be seen that since the transmitted signal consists of pairs of pulses of opposite polarity, it does not matter in which sense the core is connected to the bus, since reversal of the sense will merely result in reversal of the order of positive and negative pulses, and this will still be detected as the same but value. Also, since pulses of opposite polarities always occur in pairs, there is no net D.C. component in the signal.

Brief description of the drawings

One data processing network in accordance with the invention will now be described by way of example with reference to the accompanying drawings of which:

Figure 1 is a schematic diagram of the network,

Figure 2 shows the form of coding used for transmission of data,

Figure 3 shows a transmitter circuit, and

Figure 4 shows a receiver circuit.

Description of the embodiment of the invention

General description of the system

Referring to Figure 1, the data processing network comprises a data communication bus 10 connected to a plurality of data processing stations 11 by means of transceivers 12. The bus 10 consists of a twisted pair (i.e. a pair of insulated wires, uniformly twisted together) and is terminated at each end by a terminating resistor 13. If the twisted pair has a characteristic impedance of 100 ohms, then the terminating resistors 13 are preferably both 100 ohms in value.

The data processing stations 11 may for example be central processing units, data storage units, or data display terminals. Typically, the bus 10 may be up to 1 kilometer in length.

Any of the stations 11 can send a message over the bus to any other station. Each message contains the address of the intended destination and each station compares the addresses of messages appearing on the bus with its own address, so as to decide whether to accept them. Before sending a message, the station first listens to the bus to determine whether it is free or busy. If the bus is free, the station starts to send its message. It is possible, however, that two stations may begin to transmit messages at substantially the same time, and these messages will interfere with each other on the bus. This situation is detected by a collision detection means (not shown) in each station, which compares the outgoing message with the signal actually appearing on the bus. Any discrepancy between these two signals indicates that a collision has occurred. When a collision is detected, the station abandons transmission of the message and makes another attempt later, preferably after a random length of time to reduce the probability of a further collision.

This technique for controlling the utilisation of the bus and dealing with collisions is described in the abovementioned US Patent No. 4063220 and so will not be described in detail herein.

In the present system, the transmission rate for sending data over the bus is chosen to be 1 MHz so that each bit occupies a bit-time of 1 microsecond. Timing is by accurate clocks in each station.

Data transmission code

Referring to Figure 2, this shows schematically the form of signals on the bus. As can be seen, a binary "0" is represented by a positive pulse immediately followed by a negative pulse of the same area. A binary "1" is represented by the absence of any signal. (Of course, the opposite convention could have been used, with "1" represented by a positive/negative pulse pair).

This form of code has the advantage that it has no DC component. Moreover, if signals are detected by sensing their positive portions only, the polarity of connection of the transceivers to the bus does not matter since an inverted pulse pair is still detected in the same manner (although detection is delayed by one half bit-time). This is a useful feature since it makes it easier to connect the transceivers to the bus.

Another advantage of this code is that, since there is no power transmitted for a "1", it is possible for a station to detect a "0" from another station while the first station is transmitting a "1". This simplifies collision detection.

Each transceiver 12 comprises a transmitter circuit and a receiver circuit, described below with reference to Figures 3 and 4. The transmitter and receiver circuits are coupled to the twisted pair 10 by means of two separate ferrite cores, referred to as the transmitter and receiver cores. Each core consists of an E-shaped part, the central limb of which is threaded through the twisted pair 10, and an I-shaped part which engages with the E-shaped part to complete the magnetic circuit. The central limb of each core carries one or more windings, as will be described.

The cores and their windings are encapsulated to protect them and are housed in a shielding enclosure connected to zero potential. The enclosure also holds the transmitter and receiver circuits.

Transmitter circuit

Referring to Figure 3, this shows the transmitter core 20 and the transmitter circuit 21. The transmitter core carries two transmitter windings 23, 24, each of two turns, and an eight-turn clamping winding 25.

The transmitter winding 23 has one end connected by way of a resistor 26 to a +5 volt supply, and also to one terminal of a 100 microfarad capacitor 27, the other terminal of which is connected to earth. The other end of this winding 23 is connected to the collector of a switching transistor 28, the emitter of which is connected to earth. The other transmitter winding 24 has one end connected to earth and the other end connected to one terminal of a 1 microfarad capacitor 29, the other terminal of which is connected to the collector of the transistor 54. The opposite ends of the winding 23, 24 are connected by a diode 30.

In the quiescent state, i.e. when no pulses are being transmitted, the transistor 28 is turned off, and hence both capacitors 27, 29 are charged up to +5 volts. In order to send a positive pulse, the transistor 28 is turned on, and this causes a current of about 5mA to flow through both windings 23,24. Since the transformer ratio is 2:1, this pulse is transformed into a pulse of about 20mA on the twisted pair 10. The current is mainly drawn from the two capacitors 27, 29. At this time, the diode 30 is reverse biassed and hence does not conduct.

At the end of the positive pulse, the transistor 28 is turned off, and a backswing now occurs which produces a negative pulse as required (see Figure 2). During the backswing, the magnetic energy stored in the core produces an electromotive force across the transmitter windings which tends to keep the current flowing. This causes the diode 30 to become forward biassed, so that it now conducts current from the winding 23 into the capacitor 29 and from the winding 24 into the capacitor 27 recharging both capacitors. In this way, energy from the backswing of each pulse is recovered and used to re-charge the capacitors, instead of being wasted. This helps to reduce the power consumption of the transmitter.

A 150 picofarad capacitor 31 connected across the transistor 28 acts as an edge moderator to reduce high frequency components in the transmitted signal.

The two ends of the clamping winding 25 are connected by way of diodes 32, 33 to the 5 volt supply line, and also to a junction field-effect transistor (JFET) 34, the gate of which is connected to a pair of transistors 35, 36. In operation, when the transmitter circuit is transmitting a signal, the transistors 35, 36 turn the JFET 34 off, causing the clamping winding 25 to be open-circuited. However, when the transmitter is quiescent, or if the 5 volt power supply is turned off, the JFET 34 is turned on, causing the clamping winding to be effectively short circuited. This ensures that the transmitter circuit does not draw too much power from the bus when it is not transmitting.

Typical values for the various resistors shown in Figure 3 are as follows:

Resistor	Value (ohms)
26	10
37	22K
38	10K
39	1K
40	47
41	100K

Receiver circuit

Referring now to Figure 4, this shows the receiver core 50 and the receiver circuit 51. The receiver core carries a receiver winding 52 of eight turns. A 33 nanofarad capacitor 53 connected across this winding acts as a high frequency filter to reduce high frequency components in the received signal.

One end of the receiver winding 52 is connected by way of a 33 nanofarad capacitor 54 to the input of an amplifier 55, to produce the output signal for the receiver. This amplifier may for example be a National Semiconductor type LM311 operational amplifier. Biassing current for this amplifier is supplied by a current mirror arrangement consisting of two matched transistors 56, 57, which also provide a first stage of amplification.

Typical values for the various resistors shown in Figure 4 are as follows.

Resistors	Value (ohms)
58	5
59	5K
60	1.5K
61	220K
62	5K
63	10K

Message preamble

Whenever a station sends a message, it starts with a preamble consisting of six eight-bit bytes. The first three bytes are as follows:-

0000 0001

1110 0011

1100 0000

Each of the last three bytes has one of the following forms:

1111 1110

1111 1011

1110 1111

1011 1111

The first three bytes provide a synchronisation pattern which enables a receiving station to lock its internal clock on to the phase of the received signals and to determine the byte boundaries of the message.

The last three bytes of the preamble provide a "signature" for the message. It will be seen that each of these last three bytes consists of a single "0" in one of four possible locations (they can occur only in alternate bit locations). Thus, there are 4×4×4 = 64 different possible signatures. It is therefore possible to provide a different signature for each station, assuming there are fewer than 64 stations in the network.

The purpose of the signature is to ensure that a collision is detected even in the case where, by chance, an incoming message arrives in substantially perfect synchronism with an outgoing message. Because the signature patterns of the two messages must be different, it will be apparent that at least one of the "0" pulses of the signature of the incoming message will fall in a gap ("1") in the signature of the outgoing message. Moreover, because the "0" pulses in the signature pattern occur only at alternate bit positions, the collision can be detected even though the receiver has a dead period of one bit-time following transmission of a pulse during which it cannot detect incoming pulses.

In a modification, instead of having a unique signature for each station, each station could be arranged to generate a signature at random for each message sent by it. This might be more convenient since it would not then be necessary to assign unique signatures to the stations. There would, of course, be a possibility that two messages arriving in perfect synchronism would have identical signatures, so that a collision could not be detected at the preamble stage. However, the probability of this is very low.

It can be shown that the preamble format specified above enables collisions to be detected for any degree of overlap between incoming and outgoing messages from −19 bit-times to +46 bit-times. That is to say, if an incoming preamble is superimposed upon an outgoing preamble with any degree of misalignment within the limits stated, at least one pulse ("0") from the preamble of the incoming message will fall within a gap ("1") of the outgoing message, outside the one-bit-time dead period following an outgoing pulse. This range of detectable overlap is found to be greater than the range which can actually occur in practice, and therefore this preamble format ensures that overlapping messages will always be detected by collisions between their preambles.

CLAIMS

1. A data processing network comprising:
(a) a plurality of data processing stations;
(b) a common bus interconnecting the stations; and
(c) means for inductively coupling each station to the bus to allow the stations to communicate with one another over the bus;
(d) wherein each station has transmitter means for transmitting data over the bus in a binary-coded form in which one bit value is represented by a pulse immediately followed by a pulse of opposite polarity, and the other bit value is represented by the absence of any pulse.

2. A network according to Claim 1 wherein the means for inductively coupling a station to the bus includes a magnetic core with two transmitter windings, and the transmitter means includes
(a) two capacitors in series with the respective transmitter windings;
(b) means for charging the capacitors;
(c) switching means for completing first circuit paths allowing the capacitors to be discharged through the respective transmitter windings thereby producing an output pulse on the bus; and
(d) a diode connected between the two transmitter windings so as to be non-conducting when the capacitors are being discharged, wherein, when the switching means is turned off, the induced electromotive forces in the two transmitter windings cause the diode to conduct, thereby completing second circuit paths allowing the capacitors to be charged by currents from the transmitter windings.

3. A network according to Claim 1 or 2, wherein the means for inductively coupling each station to the bus comprises two separate magnetic cores for transmission and reception.

4. A network according to Claim 3 wherein the magnetic core for transmission has a clamping winding with a junction field-effect transistor connected across it, and means operative when the transmitter means is quiescent to cause the junction field-effect transistor to become conducting, thereby effectively short-circuiting the clamping winding.

5. A network according to any preceding claim wherein the bus comprises a twisted pair of wires.

6. A data processing network according to any preceding claim, wherein each station is arranged to include at the start of each message sent by it over the bus a preamble comprising a synchronisation pattern which is the same for all stations, and a signature pattern which differs from one station to another, the signature pattern being such that if any two such patterns are superimposed at least one pulse from each pattern will fall in a gap in the other pattern.

7. A data processing network substantially as hereinbefore described with reference to the accompanying drawings.

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